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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/023,172	02/13/98	HOLMAN T	042390.P5659

LM02/0913

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EXAMINER	
VERBRUGGE,K	
ART UNIT	**PAPER NUMBER**
2751	7

DATE MAILED: 09/13/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

See the attached non-final office action

Office Action Summary

Application No.	Applicant(s)
09/023,172	Holman
Examiner	**Group Art Unit**
Kevin Verbrugge	2751

☒ Responsive to communication(s) filed on *Aug 9, 1999*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-14* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-14* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informality: four serial numbers are missing on page 2 of the specification. Appropriate correction is required.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The abstract of the disclosure is objected to because it is not clear to the Examiner what is meant by the phrase "system memory module" in line 3. Perhaps Applicants intended --system memory controller--. Appropriate correction or clarification is required.

Claim Objections

4. Claims 1, 12, and 13 are objected to because of the following informalities:

It is not clear to the Examiner what is meant by the phrase "system memory module" in lines 2 and 3 of each claim. Perhaps

Applicants intended --system memory controller--. Appropriate correction or clarification is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by "Memory Systems Design and Applications", edited by Dave Bursky, pp. 213-220.

Regarding claims 1, 2, and 12-14, on page 217 Bursky teaches in the photo caption that "System costs plummet when function duplication is designed out. <u>While most minis duplicate read/write and control electronics for each board of memory DIPs</u>, Interdata makes one read/write/control set serve more memory, by using eight little 'daughter boards.' This packaging also simplifies reconfiguration and speeds up field repair" (emphasis added).

Furthermore, on page 219, third column, he writes that "The PC-board economy is possible through the use of 'daughter boards,' strips that are 8 in. long, 1 in. wide and plug into the 15x15 in. memory board itself. Not only does this mean that 256 kbytes can be packed on the board instead of 32 or 64 kbytes, it also means that function duplication is cut back. As a result, the read/write control logic that would have been duplicated on a series of 64-kbyte boards appears just once on the 15x15 in. motherboard, serving all 256 kbytes. Larry MacPherson, Interdata product manager for the Series Sixteen, points out that this unusual modularity makes it easy to add and subtract memory in the field, and slashes the cost of incremental memory increases" (emphasis added).

Bursky's focus in the passages above is toward the daughter card system of Interdata. However, the underlined passages above teach that it was known to use memory controllers on individual memory modules, each of which contained a plurality of memory devices as claimed. In fact, such a design appears to have been the norm. The passages above describe a new (for the time) method of reducing the duplication of the memory controllers by removing them from the memory modules and using a single controller on the motherboard for all memory modules (daughter cards). This is the norm today, and is the admitted prior art of

the instant application. However, in 1980 and before, it was common to include the memory controller on each memory module as taught above.

Bursky does not explicitly teach that the memory module controller reformats the transactions it receives before passing them on to the plurality of memory devices, however such reformatting is inherent in the devices described by Bursky since memory devices required different format signals than memory module controllers. Bursky does not characterize the memory controllers of the memory modules other than to call them read/write/control logic, which meets the broad claim language of handling requests (reads or writes) and controlling transactions.

Regarding claims 3, 4, 5, and 7, the claimed second memory bus is inherent in the memory modules since the module controller must be able to communicate with the plurality of memory devices on the module through electrical wires (bus) including address, data, and control lines, which were commonly multiplexed at the time of the invention. It would have been obvious to one skilled in the art to multiplex the bus to save signal lines.

Regarding claim 6, the bus would necessarily include a handshake signal to regulate accesses to the memory in an asynchronous system.

Regarding claims 8-10, Bursky does not mention the claimed buffers, however such elements are inherent in his memory module controller, since the controller certainly was able to hold signals it received from the system bus and transmit them on the module bus to the memory devices at the appropriate times and vice versa, in effect "buffering" the commands.

Regarding claim 11, the controller of Bursky would necessarily include a clock generator and the bus would necessarily include a clock signal to regulate accesses to the memory in a synchronous system.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/023170 and claims 1-17 of copending Application No. 09/023234. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Claims 1-20 of 09/023170 are directed to a memory module having memory devices and a memory module controller. A system memory controller is connected to the memory module controller with a memory bus.

Claims 1-14 of 09/023172 are directed to a memory module having memory devices and a memory module controller. A system memory controller (or a system memory module) is connected to the memory module controller with a memory bus. The memory module controller comprises interface circuitry to receive transactions

from the memory bus and further comprises control logic to generate other transactions for the memory devices.

The memory module controller of 09/023170 necessarily includes interface circuitry to receive transactions from the memory bus and further necessarily includes control logic to generate other transactions for the memory devices, therefore 09/023170 is not patentably distinct from 09/023172.

Claims 1-17 of 09/023234 are directed to a memory module having memory devices and a memory module controller.

The memory module of 09/023234 is necessarily connected to a system memory controller of some sort (a special chip or the CPU) with a memory bus and the memory module controller necessarily includes interface circuitry to receive transactions from the memory bus and further necessarily includes control logic to generate other transactions for the memory devices, therefore 09/023172 is not patentably distinct from 09/023234.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Kevin Verbrugge by phone at (703) 308-6663.

Any formal response to this action intended for entry should be mailed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 308-9051 or -9052 and labeled "FORMAL" or "OFFICIAL". Any informal or draft communication should be faxed to (703) 308-5359 and labeled "INFORMAL" or "UNOFFICIAL" or "DRAFT" or "PROPOSED" and followed by a phone call to the Examiner at the above number. Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Kevin Verbrugge

Patent Examiner

September 8, 1999

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER